In the Drawings

A "Replacement Sheet" is attached which includes a clean version of amended Figure 3. The attached sheet replaces the original sheet including Figure 3.

Figure 3 was amended to include the reference label "761" and to correctly place reference label "741".

REMARKS

In response to the Office Action mailed February 25, 2005, Applicant respectfully requests reconsideration. Claims 1-12 were previously pending in this application. By this amendment, Applicant is canceling claim 2 without prejudice or disclaimer. Claims 1, 3, 6, 9, and 11 have been amended. No new claims have been added. As a result, claims 1 and 3-12 are pending for examination with claims 1, 3, 6, 8, 9, and 11 being independent. No new matter has been added.

Objections to the Drawings

The Office Action objects to figure 3 for not including reference label "761" and for misplacing reference label "741". Figure 3 has been amended to include reference label "761" and correctly place reference label "741".

Accordingly, withdrawal of this objection is respectfully requested.

Objections to the Specification

The Office Action objects to the Abstract for not being in narrative form and for using legal phraseology. The Abstract has been amended and is now in accordance with MPEP § 608.01(b).

Accordingly, withdrawal of this objection is respectfully requested.

Claim Objections

The Office Action objects to claim 1 for not separating the limitations of the claim by a line indentation. Claim 1 has been amended to separate the limitations of the claim by a line indentation and is now in accordance with MPEP § 608.01(m).

Accordingly, withdrawal of the objection of claim 1 is respectfully requested.

Rejections under 35 U.S.C. §112

The Office Action rejects claims 2-7 under 35 U.S.C. §112 for being indefinite for failing to particularly point out and distinctly claim the subject matter.

The Office Actions rejects to claims 2-5 for being indefinite and/or failing to provide sufficient antecedent basis. Claim 2 has been canceled and therefore this rejection should now be moot. The term "said universal bus" in claim 3 has been amended to "a universal bus" to provide sufficient antecedent basis. The Office Action rejects claim 4 for being dependent on a rejected base claim. With the amendment of claim 3, the rejection of claim 4 should now be moot.

The Office Action rejects to claims 6 and 7 for claim 6 not providing sufficient antecedent basis for the term "The combination". Claim 6 has been amended to "A combination", therefore providing sufficient antecedent basis.

These amendments are for clarification only and do not narrow the scope of the claims.

Accordingly, withdrawal of the rejection of claims 2-7 under 35 U.S.C. §112 is respectfully requested.

Rejections Under 35 U.S.C. §102

The Office Action rejects claims 1-5 under 35 U.S.C. §102 as purportedly being anticipated by Silverman et al., U.S. Patent No. 6,370,603 (Silverman). Applicant respectfully traverses this rejection.

Silverman illustrates an interface device which enables communication between devices having disparate protocols (abstract). In a "smart" cable embodiment, shown in figure 8A (relied upon by the Office Action), Silverman describes a device including translation circuitry used to interface two other devices employing two different communications protocols (Col. 10, lines 40-43). The "smart" cable device includes first and second plastic connectors 814 and 818, respectively, a physical interface 804, USB MAC 806 and surface mount or small devices 808a-808d. In a separate embodiment, Silverman describes a single chip USB controller depicted in figure 4 (relied upon by the Office Action). The USB controller 402 includes an external memory interface 434 used to interact with *external* RAM or DRAM (Col. 7, lines 60-62). The USB controller also includes a universal asynchronous receive/transmit circuit UART 444.

Silverman does not teach or suggest combining the embodiments of figure 8A with the embodiments of figure 4.

Amended claim 1 is directed towards a communication device for a target integrated circuit chip having a digital processor, an on-chip emulator for controlling said digital processor and for collecting operation data from said digital processor for communicating to off-chip circuitry, and a target on-chip universal serial bus interface connected to said on-chip emulator, the communication device comprising an Ethernet port, a universal serial bus port, and a further integrated circuit chip having on-chip processing circuitry, on-chip memory circuitry, an on-chip memory interface for connection to memory in said device but external to the further integrated circuit chip, an on-chip Ethernet interface, and an on-chip universal serial bus interface, said on-chip Ethernet interface being connected to said Ethernet port, the said Ethernet and universal serial bus interfaces being connected to said processing circuitry for translating between Ethernet protocol data on an Ethernet bus connected to said Ethernet port and universal serial bus data for said target on-chip universal serial bus interface.

Silverman does not teach or suggest an on-chip memory interface for connection to memory *in said device* but external to the further integrated circuit chip, as recited in claim 1. As described above, Silverman instead teaches an external memory interface for connecting with *external* RAM or DRAM (Col. 7, lines 60-62).

Accordingly, claim 1 distinguishes over Silverman and withdrawal of the rejection under 35 U.S.C. §102 is respectfully requested.

Claim 3 has been amended and is now in independent form. Amended claim 3 is directed towards a communication device for a target integrated circuit chip having a digital processor, an on-chip emulator for controlling said digital processor and for collecting operation data from said digital processor and for communicating to off-chip circuitry, and a target on-chip universal serial bus interface connected to said on-chip emulator, the communication device comprising an Ethernet port, a universal serial bus port and a further integrated circuit chip having on-chip processing circuitry, on-chip memory circuitry, modem circuitry for connection of a telephone line to a universal serial bus, on-chip Ethernet interface and an on-chip universal serial bus interface, said on-chip Ethernet interface being connected to said Ethernet port, the said interfaces being connected to said processing circuitry for translating between Ethernet protocol

data on an Ethernet bus connected to said Ethernet port and universal serial bus data for said target on-chip universal serial bus interface.

Silverman does not teach or suggest an Ethernet port, a universal serial bus port and a further integrated circuit chip having on-chip processing circuitry, on-chip memory circuitry, *and* modem circuitry for connection of a telephone line to a universal serial bus, as recited in claim 3. As described above, Silverman teaches a "smart" cable device including first and second plastic connectors 814 and 818, respectively, a physical interface 804, USB MAC 806 and surface mount or small devices 808a-808d (Figure 8A). In a *separate* embodiment, Silverman teaches a USB controller including a universal asynchronous receive/transmit circuit UART 444 (Figure 4). The Office Action alleges an Ethernet port, a universal serial bus port and a further integrated circuit chip having on-chip processing circuitry and an on-chip memory circuitry are found in the embodiment depicted in figure 8A. The Office Action also alleges modem circuitry for connection of a telephone line is found in the embodiment depicted in figure 4. Even if the two embodiments contained all the limitations of claim 13 (which Applicant does not concede), a combination of the two embodiments would be improper since Silverman does not teach or suggest such a combination.

Accordingly, claim 3 distinguishes over Silverman. Claims 4 and 5 depend from claim 3 and are patentable for at least the same reasons.

Rejections Under 35 U.S.C. §103

Rejections Under 35 U.S.C. §103 over the Combination of Klaas and Silverman:

The Office Action rejects claims 6-8 under 35 U.S.C. §103(a) as purportedly being unpatentable over Klaas, U.S. Patent No. 6816750 (Klaas) in view of Silverman. Applicant respectfully traverses the rejection.

Klaas illustrates a system fabricated on a single integrated chip, which is depicted in figure 1 (relied up on by the Office Action). The system described by Klaas includes a JTAG/TIC interface 110. The JTAG part of the interface takes advantage of an ARM Multi_ICE in-circuit emulator while the TIC portion of the interface utilizes an ARM Test Interface Controller, which is a bus master on AMBA bus 102 and allows an off-chip testing device access

to the AMBA peripherals (Col. 16, lines 54 -65). The device described by Klaas also includes a USB controller 111 which is configured for three root hub ports and includes an integrated transceiver (Col. 16, lines 66-67). Klaas does not teach or suggest a connection between the in-circuit emulator and the USB host of any kind.

Claim 8 is directed towards a method of communicating with a target integrated circuit chip having a digital processor, an on-chip emulator for controlling said digital processor and for collecting operation data from said digital processor for communicating to off-chip circuitry, and a target on-chip universal serial bus interface connected to said on-chip emulator. The method comprising supplying data from said off-chip circuitry via an Ethernet bus to an Ethernet port of a communication device comprising a further integrated circuit chip having on-chip Ethernet interface circuitry and on-chip processing circuitry, passing said data as an input said Ethernet interface circuitry, in said Ethernet interface circuitry, translating said data into a form suitable for said on-chip processing circuitry, supplying said translated data to said on-chip processing circuitry, processing said translated data to provide output data, applying said output data to an on-chip universal serial bus interface, for transfer via a universal serial bus to said on-chip emulator of said target integrated circuit chip.

The combination of Klaas and Silverman does not teach or suggest applying said output data to an on-chip universal serial bus interface, for transfer via a universal serial bus to said on-chip emulator of said target integrated circuit chip, as recited in claim 8. As discussed above, Klaas instead teaches an in-circuit emulator which is accessible via a JTAG interface (Col. 16, lines 54 -65).

Accordingly, claim 8 patentably distinguishes over any combination of Klaas and Silverman and is in allowable condition.

Amended claim 6 is directed towards a combination of a communication device and a target integrated circuit chip, said target integrated circuit chip having a digital processor, an on-chip emulator for controlling said digital processor and for collecting operation data from said digital processor for communicating to off-chip circuitry, and a target on-chip universal serial bus interface connected to said on-chip emulator, the communication device comprising an Ethernet port for connection to said off-chip circuitry, a universal serial bus port and a further integrated circuit chip having on-chip processing circuitry, on-chip memory circuitry, an on-chip Ethernet interface and an on-chip universal serial bus interface, said on-chip Ethernet interface

being connected to said Ethernet port, the said interfaces being connected to said processing circuitry for translating between Ethernet protocol data on an Ethernet bus connected to said Ethernet port and universal serial bus data for said target on-chip universal serial bus interface, wherein the on-chip emulator is connected to the communication device via a universal serial bus.

As should be appreciated from the above discussion relating to claim 8, the combination of Silverman and Klaas does not teach or suggest a target on-chip universal serial bus interface connected to said on-chip emulator, as recited in claim 6.

Accordingly, claim 6 patentably distinguishes over any combination of Klaas and Silverman and is in allowable condition. Claim 7 depends from claim 6 and is patentable for at least the same reasons.

Rejections Under 35 U.S.C. §103 over the Combination of Silverman, Klaas, and Swoboda:

The Office Action rejects claims 9-12 under 35 U.S.C. §103(a) as purportedly being unpatentable over Silverman in view of Klaas and further in view of Swoboda, U.S. Patent Application Publication No. 2002/0059541 A1 (Swoboda). Applicant respectfully traverses the rejection.

Swoboda illustrates how connectivity between an emulation controller and a plurality of target devices may be automatically detected (abstract). Swoboda describes an off-chip emulator which acts as a bridge between a host computer and a target system, handling all debug information passed between the debugger application running on the host computer and a target application executing on a target processor ([0069]). Swoboda teaches an Ethernet 10T and 100T, TCP/IP protocol and a USB may be used to connect a host computer to an off-chip emulator ([0065] and [0066]).

Amended claim 9 is directed towards a method of debugging a target integrated circuit chip using a host computer device, said target integrated circuit having a digital processor and an on-chip emulator wherein said on-chip emulator is operable to control said digital processor according to a host program and to collect operation data from said digital processor for communicating to said host, said chip comprising a target on-chip universal serial bus interface connected to said on-chip emulator. The method comprising providing a communication device comprising an Ethernet port, a universal serial bus port and a further integrated circuit chip

having on-chip processing circuitry, on-chip memory circuitry, an on-chip Ethernet interface and an on-chip universal serial bus interface, connecting said Ethernet port to said host via an Ethernet link, connecting said communication device to said target on-chip universal serial bus interface and said on-chip emulator via a universal serial bus, communicating data between said on-chip emulator and said on-chip processing circuitry, processing data in said on-chip processing circuitry to provide output data, and supplying said output data to said host via said Ethernet port.

As should be appreciated from the above discussion relating to claim 8, the combination of Silverman, Klaas, and Swoboda does not teach or suggest connecting said communication device to said target on-chip universal serial bus interface and said on-chip emulator via a universal serial bus, as recited in claim 9.

Accordingly, claim 9 patentably distinguishes over any combination of Silverman, Klaas and Swoboda, and is in allowable condition. Claims 10 and 12 depend on claim 9 and are patentable for at least the same reasons.

Claim 11 has been amended to include the limitation discussed above in relation to claim 8. Amended claim 11 is directed towards a method of debugging a target integrated circuit having a digital processor and an on-chip emulator wherein said on-chip emulator is operable to control said digital processor and to collect operation data from said digital processor for communicating to a host, said chip comprising a target on-chip universal serial bus interface connected to said on-chip emulator, the method comprising providing a communication device comprising an Ethernet port, a universal serial bus port and a further integrated circuit chip having on-chip processing circuitry, on-chip memory circuitry, an on-chip Ethernet interface and an on-chip universal serial bus interface, connecting said Ethernet port to said host, connecting said communication device to said target on-chip universal serial bus interface and said on-chip emulator via a universal serial bus, communicating data between said on-chip emulator and said on-chip processing circuitry, processing said data in said on-chip processing circuitry to provide output data, supplying said output data to said on-chip emulator circuitry.

As should be appreciated from the above discussion relating to claim 8, the combination of Silverman, Klaas, and Swoboda does not teach or suggest connecting said communication device to said target on-chip universal serial bus interface and said on-chip emulator via a universal serial bus, as recited in claim 11.

Accordingly, claim 11 patentably distinguishes over any combination of Silverman, Klaas and Swoboda, and is in allowable condition.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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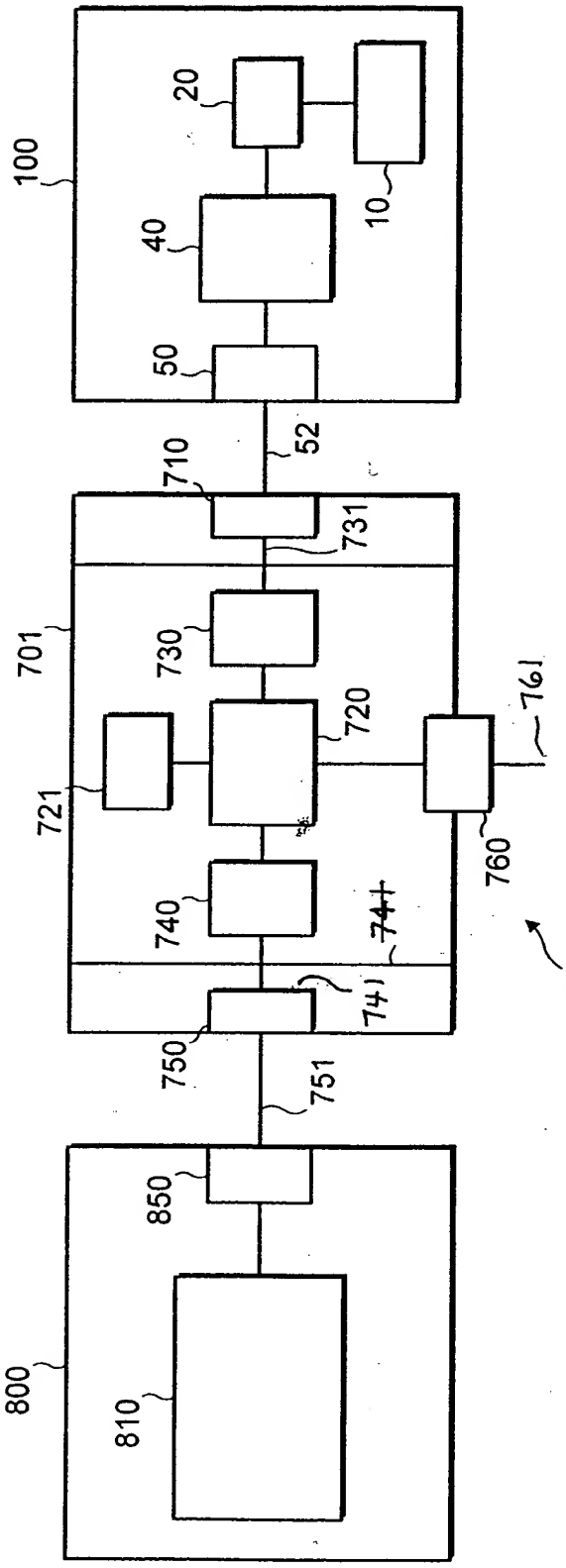

FIG. 3